

WHAT IS CLAIMED IS:

- 1 1. A ring oscillator, comprising:
 - 2 a feedback input terminal;
 - 3 a circuit output terminal for generating an oscillator output
 - 4 signal; and
 - 5 a positive feedback loop between said circuit output terminal
 - 6 and said feedback input terminal,
 - 7 said positive feedback loop including a plurality of delaying
 - 8 stages connected in cascade, and a transfer gate coupled to each of
 - 9 said plurality of delaying stages, each of said transfer gates including a
 - 10 pair of transistors of the first and second conductivity types connected
 - 11 in parallel, said transistors of the first conductivity type being
 - 12 controlled by a first control signal, said transistors of the second
 - 13 conductivity type being controlled by a second control signal.
- 1 2. The ring oscillator as claimed in claim 1, wherein said positive
- 2 feedback loop includes, as said plurality of delaying stages, an odd
- 3 number of delaying inverting stages, each of said delaying inverting
- 4 stages including a CMOS inverter, and wherein said pair of transistors
- 5 of each transfer gate are p-channel and n-channel transistors,
- 6 respectively, and wherein said ring oscillator is operable during a first
- 7 mode when said p-channel transistors are ON and said n-channel
- 8 transistors are OFF, during a second mode when said p-channel
- 9 transistors are OFF and said n-channel transistors are ON, and during
- 10 a third mode when said p-channel and n-channel transistors are both
- 11 ON.
- 1 3. The ring oscillator as claimed in claim 1, wherein said positive
- 2 feedback loop includes an NAND input stage, wherein said positive
- 3 feedback loop includes, as said plurality of delaying stages, an even
- 4 number of delaying inverting stages following said NAND input stage,
- 5 each of said delaying inverting stages including a CMOS inverter, and
- 6 wherein said first and second conductivity type transistors are

7 p-channel and n-channel transistors, respectively, and wherein said
8 ring oscillator is operable during a first mode when said p-channel
9 transistors are ON and said n-channel transistors are OFF, during a
10 second mode when said p-channel transistors are OFF and said
11 n-channel transistors are ON, and during a third mode when said
12 p-channel and n-channel transistors are both ON.

1 4. The ring oscillator as claimed in claim 2, wherein said first
2 control signal has two levels, and said second control signal has two
3 levels, and further comprising a control circuit in communication with
4 gates of said p-channel transistors and with gates of said n-channel
5 transistors for shifting said first control signal between said two levels
6 thereof and said second control signal between said two levels thereof.

1 5. The ring oscillator as claimed in claim 3, wherein said first
2 control signal has two levels, and said second control signal has two
3 levels, and further comprising a first terminal connected to gates of
4 said p-channel transistors and a second terminal connected to gates of
5 said n-channel transistors, said first and second terminals being
6 communicable with a control circuit for shifting said first control signal
7 between said two levels thereof and said second control signal
8 between said two levels thereof.

1 6. The ring oscillator as claimed in claim 1, further comprising a
2 divider in communication with said circuit output terminal and
3 operable to receive said oscillator output signal.

1 7. The ring oscillator as claimed in claim 2, further comprising a
2 divider in communication with said circuit output terminal and
3 operable to receive said oscillator output signal.

1 8. The ring oscillator as claimed in claim 3, further comprising a
2 divider in communication with said circuit output terminal and
3 operable to receive said oscillator output signal.

1 9. The ring oscillator circuit as claimed in claim 4, further
2 comprising a divider in communication with said circuit output terminal
3 and operable to receive said oscillator output signal.

1 10. The ring oscillator circuit as claimed in claim 5, further
2 comprising a divider in communication with said circuit output terminal
3 and operable to receive said oscillator output signal.

1 11. A semiconductor integrated circuit comprising said ring
2 oscillator as claimed in claim 1.

1 12. The semiconductor integrated circuit as claimed in claim 11,
2 wherein said positive feedback loop includes, as said plurality of
3 delaying stages, an odd number of delaying inverting stages, each of
4 said delaying inverting stages including a CMOS inverter, and wherein
5 said pair of transistors of each transfer gate are p-channel and
6 n-channel transistors, respectively, and wherein said ring oscillator is
7 operable during a first mode when said p-channel transistors are ON
8 and said n-channel transistors are OFF, during a second mode when
9 said p-channel transistors are OFF and said n-channel transistors are
10 ON, and during a third mode when said p-channel and n-channel
11 transistors are both ON.

1 13. The semiconductor integrated circuit as claimed in claim 11,
2 wherein said positive feedback loop includes an NAND input stage,
3 wherein said positive feedback loop includes, as said plurality of
4 delaying stages, an even number of delaying inverting stages
5 following said NAND input stage, each of said delaying inverting stages
6 including a CMOS inverter, and wherein said first and second
7 conductivity type transistors are p-channel and n-channel transistors,
8 respectively, and wherein said ring oscillator is operable during a first
9 mode when said p-channel transistors are ON and said n-channel
10 transistors are OFF, during a second mode when said p-channel
11 transistors are OFF and said n-channel transistors are ON, and during

12 a third mode when said p-channel and n-channel transistors are both
13 ON.

1 14. The semiconductor integrated circuit as claimed in claim 12,
2 wherein said first control signal has two levels, and said second control
3 signal has two levels, and further comprising a first terminal connected
4 to gates of said p-channel transistors and a second terminal connected
5 to gates of said n-channel transistors, said first and second terminals
6 being communicable with a control circuit for shifting said first control
7 signal between said two levels thereof and said second control signal
8 between said two levels thereof.

1 15. The semiconductor integrated circuit as claimed in claim 13,
2 wherein said first control signal has two levels, and said second control
3 signal has two levels, and further comprising a first terminal connected
4 to gates of said p-channel transistors and a second terminal connected
5 to gates of said n-channel transistors, said first and second terminals
6 being communicable with a control circuit for shifting said first control
7 signal between said two levels thereof and said second control signal
8 between said two levels thereof.

1 16. The semiconductor integrated circuit as claimed in claim 11,
2 further comprising a divider in communication with said circuit output
3 terminal and operable to receive said oscillator output signal.

1 17. The semiconductor integrated circuit as claimed in claim 12,
2 further comprising a divider in communication with said circuit output
3 terminal and operable to receive said oscillator output signal.

1 18. The semiconductor integrated circuit as claimed in claim 13,
2 further comprising a divider in communication with said circuit output
3 terminal and operable to receive said oscillator output signal.

1 19. The semiconductor integrated circuit as claimed in claim 14,

2 further comprising a divider in communication with said circuit output
3 terminal and operable to receive said oscillator output signal.

1 20. The semiconductor integrated circuit as claimed in claim 15,
2 further comprising a divider in communication with said circuit output
3 terminal and operable to receive said oscillator output signal.

1 21. The ring oscillator as claimed in claim 2, wherein each of said
2 transfer gates is coupled to the input of one of said CMOS inverters
3 that follow said transfer gate.

1 22. The ring oscillator as claimed in claim 3, wherein each of said
2 transfer gates is coupled to the input of one of said CMOS inverters
3 that follow said transfer gate, and wherein said NAND input stage is
4 coupled to one of said transfer gates that follow.

1 23. A test method for verifying fabrication of transistors in an
2 integrated circuit, comprising:

3 providing a ring oscillator on a die under test during fabrication
4 of said die, said ring oscillator including a plurality of delaying stages
5 connected in cascade, and a transfer gate coupled to each of said
6 plurality of delaying stages, each of said transfer gates including a pair
7 of transistors of the first and second conductivity types connected in
8 parallel, said transistors of the first conductivity type and said
9 transistors of the second conductivity type being fabricated by same
10 processes as transistors of the first conductivity type and transistors
11 of the second conductivity type constituting an integrated circuit on
12 said die;

13 measuring a first period of said ring oscillator by operating said
14 ring oscillator to provide a first oscillator output signal during a first
15 mode when said transistors of the first conductivity type of each of
16 said transfer gates are ON and said transistors of the second
17 conductivity type of each of said transfer gates are OFF;

18 measuring a second period of said ring oscillator by operating

19 said ring oscillator to provide a second oscillator output signal during a
20 second mode when said transistors of the first conductivity type of
21 each of said transfer gates are OFF and said transistors of the second
22 conductivity type of each of said transfer gates are ON;

23 measuring a third period of said ring oscillator by operating said
24 ring oscillator to provide a third oscillator output signal during a third
25 mode when said transistors of the first conductivity type of each of
26 said transfer gates are ON and said transistors of the second
27 conductivity type of each of said transfer gates are ON; and

28 analyzing said first, second and third periods for decision
29 making on whether said integrated circuit on said die meets
30 preselected specification.

1 24. The test method as claimed in claim 23, wherein said step of
2 analyzing includes the steps of:

3 comparing said first period with a first preselected specification;

4 comparing said second period with a second preselected
5 specification; and

6 comparing said third period with a third preselected
7 specification.

1 25. The test method as claimed in claim 23, wherein the total
2 number of said plurality of delaying stages is odd, wherein each of said
3 delaying stages includes a CMOS inverter, and wherein said pair of
4 transistors of each transfer gate are p-channel and n-channel
5 transistors, respectively.

1 26. The test method as claimed in claim 23, wherein said ring
2 oscillator includes an NAND input stage, wherein the total number of
3 said plurality of delaying stages is even, and wherein each of said
4 delaying stages includes a CMOS inverter, and wherein said first and
5 second conductivity type transistors are p-channel and n-channel
6 transistors, respectively.

1 27. A test apparatus for verifying fabrication of transistors in an
2 integrated circuit, comprising:

3 a ring oscillator provided on a die under test during fabrication
4 of said die, said ring oscillator including a plurality of delaying stages
5 connected in cascade, and a transfer gate coupled to each of said
6 plurality of delaying stages, each of said transfer gates including a pair
7 of transistors of the first and second conductivity types connected in
8 parallel, said transistors of the first conductivity type and said
9 transistors of the second conductivity type being fabricated by same
10 processes as transistors of the first conductivity type and transistors
11 of the second conductivity type constituting an integrated circuit on
12 said die;

13 circuitry operable for measuring
14 a first period of said ring oscillator by operating said ring
15 oscillator to provide a first oscillator output signal during a first mode
16 when said transistors of the first conductivity type of each of said
17 transfer gates are ON and said transistors of the second conductivity
18 type of each of said transfer gates are OFF,

19 a second period of said ring oscillator by operating said ring
20 oscillator to provide a second oscillator output signal during a second
21 mode when said transistors of the first conductivity type of each of said
22 transfer gates are OFF and said transistors of the second conductivity
23 type of each of said transfer gates are ON, and

24 a third period of said ring oscillator by operating said ring
25 oscillator to provide a third oscillator output signal during a third mode
26 when said transistors of the first conductivity type of each of said
27 transfer gates are ON and said transistors of the second conductivity
28 type of each of said transfer gates are ON; and

29 circuitry operable for analyzing said first, second and third
30 periods for decision making on whether said integrated circuit on said
31 die meets preselected specification.

1 28. The test apparatus as claimed in claim 27, wherein said circuitry
2 operable for analyzing includes:

3 circuitry operable for comparing said first period with a first
4 preselected specification;

5 circuitry operable for comparing said second period with a
6 second preselected specification; and

7 circuitry operable for comparing said third period with a third
8 preselected specification.

1 29. A computer program product embodied in a storage media, the
2 computer program product including a program of instructions for
3 performing:

4 measuring a first period of a ring oscillator for a die under test,
5 wherein said ring oscillator is provided on said die during
6 fabrication of said die, said ring oscillator including a plurality of
7 delaying stages connected in cascade, and a transfer gate coupled to
8 each of said plurality of delaying stages, each of said transfer gates
9 including a pair of transistors of the first and second conductivity types
10 connected in parallel, said transistors of the first conductivity type and
11 said transistors of the second conductivity type being fabricated by
12 same processes as transistors of the first conductivity type and
13 transistors of the second conductivity type constituting an integrated
14 circuit on said die,

15 said step of measuring said first period being carried out by
16 operating said ring oscillator to provide a first oscillator output signal
17 during a first mode when said transistors of the first conductivity type
18 of each of said transfer gates are ON and said transistors of the second
19 conductivity type of each of said transfer gates are OFF;

20 measuring a second period of said ring oscillator by operating
21 said ring oscillator to provide a second oscillator output signal during a
22 second mode when said transistors of the first conductivity type of
23 each of said transfer gates are OFF and said transistors of the second
24 conductivity type of each of said transfer gates are ON;

25 measuring a third period of said ring oscillator by operating said
26 ring oscillator to provide a third oscillator output signal during a third
27 mode when said transistors of the first conductivity type of each of

28 said transfer gates are ON and said transistors of the second
29 conductivity type of each of said transfer gates are ON; and
30 analyzing said first, second and third periods for decision
31 making on whether said integrated circuit on said die meets
32 preselected specification.

1 30. The computer program product as claimed in claim 29, wherein
2 said step of analyzing includes:
3 comparing said first period with a first preselected specification;
4 comparing said second period with a second preselected
5 specification; and
6 comparing said third period with a third preselected
7 specification.